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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Hsin-Hui Lee

Serial No. 10/ 045,783

Group Art Unit: 2827

Filed: Jan. 12, 2002

Examiner: Chambliss, Alonzo

For: Method of Making a Wafer Level Chip Scale Package

Attorney Docket No.: 67,200-591

Box Official Draftsperson
Commissioner for Patents
Alexandria, VA 22313-1450

TRANSMITTAL OF FORMAL DRAWINGS

In response to the Notice of Allowability mailed on November 17, 2003, attached please find:

(a) the formal drawing(s) for this application.

Number of Sheet(s) 5

■ Each sheet of drawing(s) indicates the identifying indicia

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CERTIFICATE OF MAILING (37 C.F.R. 1.8(a))

I hereby certify that this correspondence is being deposited with the Official Draftsperson, Commissioner for Patents, Alexandria, VA 22313-1450 on the date indicated below.

Kathy Dixon

Date: Feb. 17, 2004